

09/625119  
rcs08 u.s. pro

Jc906

130

	Subclass	ISSUE CLASSIFICATION
	Class	

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PATENT NUMBER

**U.S. UTILITY Patent Application**

<b>O.I.P.E.</b> <i>m.1t 88<sup>2</sup></i>	<b>PATENT DATE</b> <i>AA</i>
<b>SCANNED</b>	<b>O.A.</b>

APPLICATION NO. 09/625116	CONT/PRIOR D F	CLASS 257 361	SUBCLASS 56	ART UNIT 2811 7536	EXAMINER Bots Henson
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TS Isabelle Claverie

## Protection of the logic well of a component including an integrated MOS power transistor

TITLE

PTO-2040  
12/99

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	<div style="text-align: center;">(Assistant Examiner) _____ (Date) _____</div> <div style="text-align: center;">(Primary Examiner) _____ (Date) _____</div> <div style="text-align: center;">(Legal Instruments Examiner) _____ (Date) _____</div>			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____				ISSUE FEE	
<input checked="" type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				Amount Due	Date Paid
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